F4 - Logic Circuit Design Exercises

2nd Semester, 2008

Lab 13 – 14

Ben A. Abderazek
The University of Aizu
E-mail:benab@u-aizu.ac.jp

Release Date:	Jan. 14, 2009
Due Date :	Jan. 27, 2009

1 Today's Laboratory Objective

More on finite state machine design(FSM).

2 Background

For information about how to use Cadence tool, jump to the following tutorials:

- Cadence general introduction:
  `http://www.u-aizu.ac.jp/~benab/classes/ca/doc/cadence/`
- Cadence delay setting:
  `http://www.u-aizu.ac.jp/~benab/classes/ca/doc/cadence/DelaySetting.html`
- Logic circuit glossary:
  `http://www.u-aizu.ac.jp/~benab/classes/ld/doc/glossary.html`

3 Exercise 13: Traffic signal controller design

Design a traffic signal controller using Moore machine. Refer to Fig. 1. The behaviors of the controller are defined as follows:

1. This controller is used for the traffic signals at the point where a wide road and a narrow road are crossed.
2. Car detector is located to the narrow road. Car detection is informed to the controller as the input signal CD is 1.
3. There are six traffic signals. Three of them are used for the wide road. The controller generates 1 for WB, WY, and WR when they are blue, yellow, and red, respectively. The rest of traffic signals are used for the narrow road. The controller generates 1 for NB, NY, and NR when they are blue, yellow, and red, respectively. WB, WY, WR, NB, NY, and NR are considered as the outputs of the controller.

Table 1: Gates delay assumption.

TYPE	Function	DELAY
INV	Inverter	1
NAND2	2 input NAND	2
NAND3	3 input NAND	3
NOR2	2 input NOR	2
NOR3	3 input NOR	3
AND2	2 input AND	3
AND3	3 input AND	4
OR2	2 input OR	3
OR3	3 input OR	4
XOR2	2 input XOR	5
XOR3	3 input XOR	6

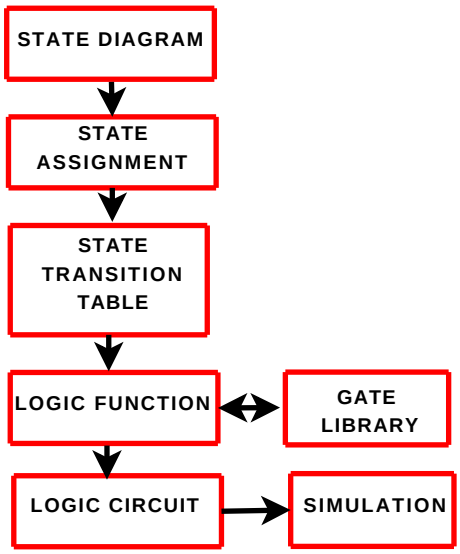

Figure 1: Lab 13 Design Flow

4. The traffic signal for the wide road becomes yellow after two cycles of car detection (CD = 1). In the next cycle, the wide road becomes red and the narrow road becomes blue. After two cycles, the narrow road becomes yellow. In the next cycle, the wide road becomes blue and the narrow road becomes red. Hint: In this controller, 7 states will be required.

5. The initial state of the controller is that the wide road is blue and the narrow road is red. Use edge-trigger DFF with a reset signal.

6. State is changed whenever a positive edge of clock signal happens

3.1 Exercise 13 Tasks

- Define inputs, outputs, and states
- Write down the state diagram (state transition graph) for the FSM
- Perform state assignment

- Write down the state transition table and output table
- Synthesize logic circuits for the state transition function and the output signals
- Draw schematic and set delay
- Decide clock cycle time
    1. Analyze the critical path delay of a circuit for the state transition function
    2. We assume setup time, hold time, and marging as 10 ns, 10 ns, and 20 ns respectively (40 ns in total).
    3. Calculate the clock cycle time as 1+2
- Write down testfixture.new so that all state transitions are simulated
- Simulate the circuit and explain the correctness of the circuit (Simulate all state transitions).

4 Report submission

4.1 Contents

Your report should be prepared in English and should contain the following:

- Your name, your ID and the Lab #.
- FSM (state diagram and mathematical representation)
- State assignment
- State transition table targeting for the master-slave DFF
- Logic functions derived from Karnaugh map
- Schematic (with delays)
- Explanation how to decide clock cycle time
- Testfixture.new
- Waveform and explanation

4.2 Submission Format

Hard Copy.

References

[1] Hiroshi Saito, Logic Circuit Design Course Web page, Second Semester, 2008.