Logic Circuit Design Exercise 11

- Purpose of this exercise

  i. You learn how to design a sequential circuit from a counter

- Assumption for gate library

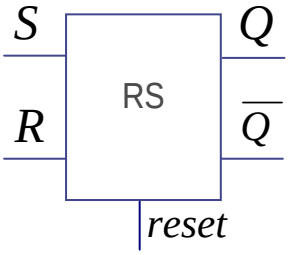
  In your designs, you can use gates specified as follows. Take corresponding gates from library "sample" and assign gate delay using property button.

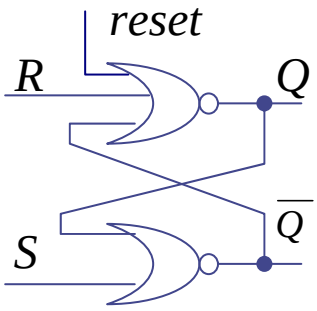
Gate lib

Name	Delay
INV	1
NAND2	2
NAND3	3
NOR2	2
NOR3	3
AND2	3
AND3	4
OR2	3
OR3	4

- Exercise 11.1 RS latch with a reset signal

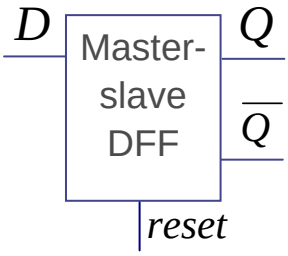
  Make an RS latch which has a "reset" signal to force Q to 0 and $\overline{Q}$ to 1 when "reset" is 1. Then set proper delay for each gate and make a symbol.

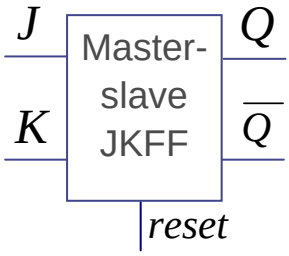




- Exercise 11.2 Master-slave DFF and JKFF with a reset signal

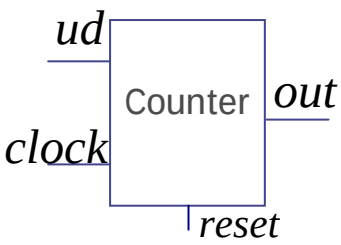
  Make new master-slave DFF and JKFF using RS latch with a reset signal. Then, set proper delay for each gate and make a symbol. Note that master-slave JKFF is an extra exercise.





- Exercise 11.3 Design of an up-down counter

  You design an up-down counter which counts up from 0 to 6 when input signal "ud" is 0 and counts down from 6 to 0 when input signal "ud" is 1.



i. “reset” signal is used to return the counter value to 0 (i.e., the initial state). In all other cases, “reset” signal must be 0.

ii. The next counter value is 0 when the counter value is 6 and “ud” is 0 while the next counter value is 6 when the counter value is 0 and “ud” is 1

iii. The output signal “out” is 1 when the counter value is 6

1. Draw state diagram and state transition table
2. Do state assignment
3. Make state transition table targeting master-slave DFF
4. Synthesize logic circuit using Karnaugh map and the given gate library
5. Draw the schematic
6. Set delay for each gate
7. Decide clock cycle time
   Note: We assume setup time, hold time, and margin as 10ns, 10ns, and 20ns
8. Write down testfixture.new to verify all state transitions
9. Simulate the circuit and explain the correctness of the circuit

- Exercise 11.4 Extra
  1. Make state transition table targeting master-slave JKFF
  2. Synthesize logic circuit using Karnaugh map and a given gate library
  3. Compare gate number and critical path delay between logic circuits in exercise 11.3 and 11.4
  4. Draw the schematic
  5. Set delay for each gate
  6. Decide clock cycle time with the same assumption as in exercise 11.3
  7. Simulation using the same testfixture.new as in exercise 11.3

- Report (Deadline is 10:40 on Jan. 8)

Prepare your report in English. The following items must be included in your report.

1. Title page: Name, ID
2. Exercise 11.1
   ① Schematic and symbol of RS latch with a reset signal
2. Exercise 11.2
   ① Schematics and symbols of master-slave DFF (and JKFF)
3. Exercise 11.3
   ① State diagram and state transition table
   ② State assignment

③ State transition table for DFF
④ Logic function derived from Karnaugh map and logic circuit
⑤ Schematic
⑥ Explanation how to decide clock cycle time
⑦ Testfixture.new
⑧ Waveform and explanation

4. Exercise 11.4
   ① State transition table for JKFF
   ② Logic function derived from Karnaugh map and logic circuit
   ③ Comparison of gate number and critical path delay
   ④ Schematic
   ⑤ Explanation how to decide clock cycle time
   ⑥ Waveform and explanation