F4 - Logic Circuit Design Exercises

2nd Semester, 2008

Lab 9

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Release Date: Dec. 3, 2008
Due Date : Dec. 10, 2008

1 Today's Laboratory Objective

Practice how to design and simulate combinational circuits.

2 Background

For information about how to use Cadence tool, jump to the following tutorials:

- Cadence general introduction:
  `http://www.u-aizu.ac.jp/~benab/classes/ca/doc/cadence/`
- Cadence delay setting:
  `http://www.u-aizu.ac.jp/~benab/classes/ca/doc/cadence/DelaySetting.html`
- Logic circuit glossary:
  `http://www.u-aizu.ac.jp/~benab/classes/ld/doc/glossary.html`

Table 1: Gates delay assumption.

TYPE	Function	DELAY
INV	Inverter	1
AND2	2 input AND	2
AND3	3 input AND	3
AND4	4 input AND	4
OR2	2 input OR	2
OR3	3 input OR	3
OR4	4 input OR	4
XOR2	2 input XOR	3
XOR3	3 input XOR	4

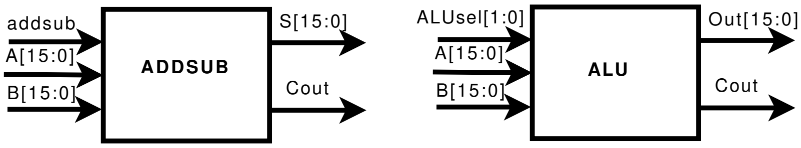
2.1 Basic Types of Digital Circuits

The basic **and**, **or**, and **not** gates can be combined in a huge variety of ways to build the digital circuitry that drives modern computers. Two basic categories of circuits are:

Combinational Circuits: Circuits whose outputs depend only on the current inputs; hence they appear to combine the inputs in some way to produce the outputs; and

Sequential Circuits: Circuits whose outputs depend on the both the current and past inputs; hence they use the sequence of inputs over time to determine the output

In this lab, we only practice the first category - *combinationa circuit*. Refer to Figure 1(a).



(a) ADDSUB input and output ports

ALUsel[1:0]	Function (Out)
00	ADD
01	SUB
10	OR
11	AND

(b) ALU input and output ports

Figure 1: ADDSUB and ALU circuits.

3 Exercise 9-1: 16-bit addition/subtraction (ADDSUB) Design

1. Use the given gate library in Table 1, the previously designed RCA and 2-to-1 MUX and draw the ADDSUB schematic.
   Note:
   - Make 16-bit 2-to-1 MUX by changing the instance name of 1-bit 2-to-1 MUX from I## to I##$< 15 : 0 >$.
   - Use 2's complement method to represent negative numbers
2. Make a symbol for ADDSUB circuit
3. Show the number of gates and the critical path delay
4. Write down testfixture to simulate the data sown in Table 2.
   Set B[15:0] to the last digit of your ID + (0230)16.
5. Simulate the circuit and verify its correctness using waveform
   Write the calculation of subtraction by hand and compare it with the one on waveform

4 Exercise 9-2: 16-bit ALU Design

Refer to Figure 1(b).

Table 2: Test sequences for Exercise 9-1 (ADDSUB).

A[15:0]	B[15:0]	addsub	S[15:0]
0101		0	
00ff		0	
0f0f		0	
ffff		0	
0101		1	
00ff		1	
0f0f		1	
ffff		1	

Table 3: Test sequences for Exercise 9-2 (ALU).

A[15:0]	B[15:0]	ALUsel[1:0]	Out[15:0]
0000		00	
0f0f		00	
ff11		00	
0000		01	
0f0f		01	
ff11		01	
0000		10	
0f0f		10	
ff11		10	
0000		11	
0f0f		11	
ff11		11	

1. Draw the schematic using the given gate library in Table 1, the previously designed ADDSUB and the 4-to-1 MUX circuits.
   Make 16-bit OR, AND, and 4-to-1 MUX by changing the instance name of 1-bit OR, AND, and $2-to-1$ MUX from I## to I##$< 15 : 0 >$
2. Make the circuit symbol
3. Show the number of gates (categorize by types) and the critical path delay
4. Write down testfixure to simulate the data shown in Table 3.
   Note: B[15:0] is the last digit of your ID + (352a)16
5. Simulate the circuit and verify the correctness on waveform.
   Write the calculation of subtraction by hand and compare it with the one on waveform.

5 Report submission

5.1 Contents

Your report should be prepared in English and should contain the following:

1. Your name, your ID and the Lab #.
2. **Exercise 9-1**
    - Schematic (with gate delay)
    - Report the number of gaets and the critical path
    - Testfixure.new
    - Waveform and explanation for correctness
3. **Exercise 9-2**
    - Schematic (with gate delay)
    - Report the number of gaets and the critical path
    - Testfixure.new
    - Waveform and explanation for correctness

5.2 Submission Format

Hard Copy.

References

[1] Hiroshi Saito, Logic Circuit Design Course Web page, Second Semester, 2008.