F4 - Logic Circuit Design Exercises

2nd Semester, 2008

Lab 6

Ben A. Abderazek
The University of Aizu
E-mail:benab@u-aizu.ac.jp

Release Date:	Nov. 5, 2008
Due Date :	Nov. 12, 2008

1 Today's Laboratory Objective

Practice how to specify gate delay, and how to identify and remove static logic hazards[1].

2 Background

For information about how to use Cadence tool, jump to the following tutorials:

- Cadence general introduction:
  `http://www.u-aizu.ac.jp/~benab/classes/ca/doc/cadence/`
- Cadence delay setting:
  `http://www.u-aizu.ac.jp/~benab/classes/ca/doc/cadence/DelaySetting.html`
- Logic circuit clossary:
  `http://www.u-aizu.ac.jp/~benab/classes/ld/doc/clossary.html`

Refer to Figure 1 for adding "td" delay to a logic gate using our *icds* tool.

3 Exercise 6

3.1 Exercise 6-1: Specifying gate delay

Refer to the table shown in Figure 2 and the logic circuit shown in Figure 3. Then, use *icds* tool and draw the schematic. Specify gate delay "td" for each gate.

3.2 Exercise 6-2: Identification of static logic hazards

In simulation, we assume single input change. There are three possibilities of static logic hazards. Identify and explain when they happen on the K map showing "start point" and "end point" of single input changes. Then, write down "testfixture.new" so that three static logic hazards happen on waveform.

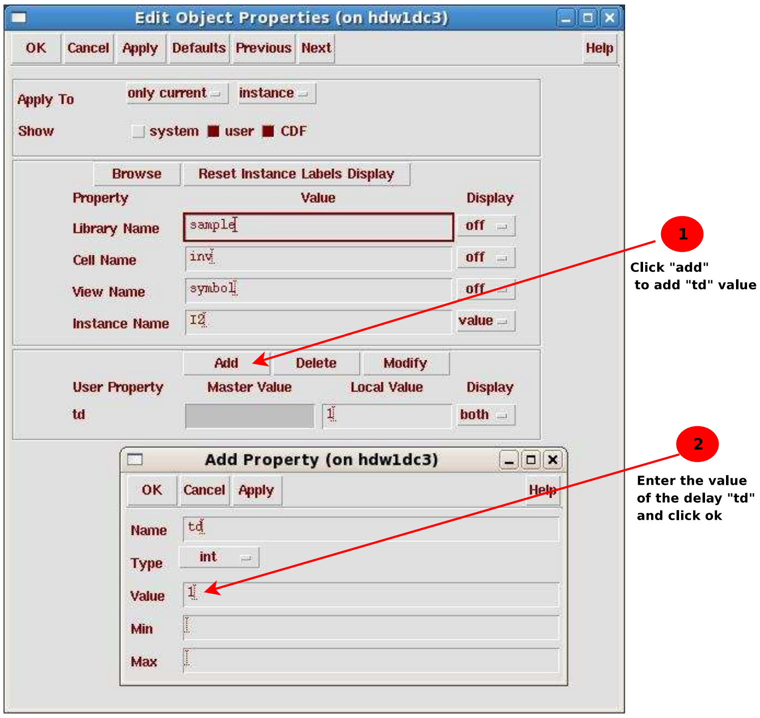

Figure 1: How to add delay to a gate.

ab/cd	00	01	11	10
00	0	1	1	0
01	0	1	1	1
11	1	1	0	1
10	0	0	0	0

Figure 2: K map.

3.3 Exercise 6-3: Removal of static hazards

Remove static logic hazards by inserting new gates. Explain why static logic hazards are removed by the insertion if new gates. Then, simulate your new circuit and confirm that there is no static logic hazard anymore on waveform.
Note: You must use the same "testfixture.new" prepared in 6-2.

4 Report submission

4.1 Contents

Your report should be prepared in English and should contain the following:

1. Your name, your ID and the Lab #.
2. **Exercise 6**

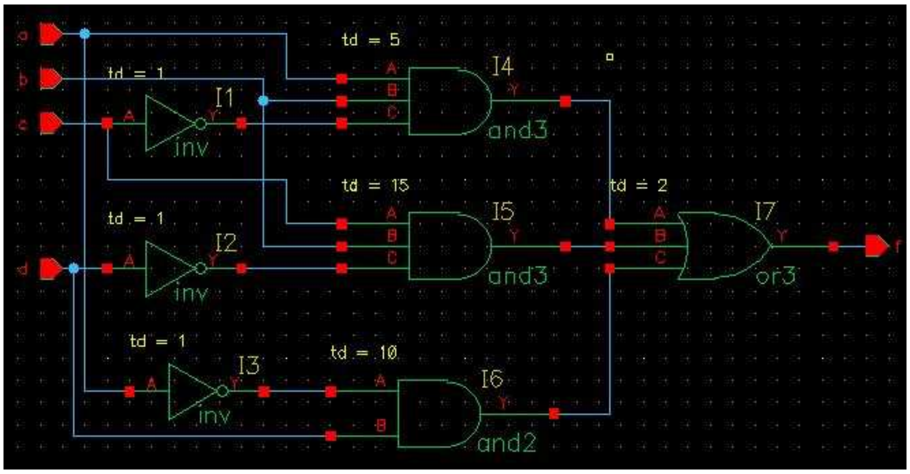

Figure 3: Logic circuit.

- Schematics (with gate delays)
- explanation of static logic hazards on K map.
- Testfixture.new
- Waveform (Explain where static logic hazards happen)
- New schematic obtained by inserting new gates
- New testfixure.new
- new waveform and explain why there is no static hazard

4.2 Submission Format

Hard Copy.

References

[1] Hiroshi Saito, Logic Circuit Design Course Web page, Second Semester, 2008.