F4 - Logic Circuit Design Exercises

2nd Semester, 2008

Lab 3

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1 Objective

Learn how to debug a logic circuit.

2 Introduction to Cadence design tool

Read the following tutorial about Cadence tool:
`http://www.u-aizu.ac.jp/~benab/classes/cs/doc/cadence/`

3 Exercise 3.1

Debugging at logic design phase.

3.1 Exercise 3.1 Tasks

1. Correct Equations 1 and 2 so that they correspond to the specification shown in Table 1.
2. Use *icds* tool and draw the corresponding logic circuit.

Table 1: Truth Table (Specification)

A	B	C	F1	F2
0	0	0	0	1
0	0	1	0	0
0	1	0	1	0
0	1	1	1	1
1	0	0	1	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

3. Simulate the circuit.

$$F1 = (\bar{A} \wedge \bar{B} \wedge \bar{C}) \vee (\bar{A} \wedge B \wedge \bar{C}) \vee (\bar{A} \wedge B \wedge C) \vee (A \wedge B \wedge \bar{C}) \vee (A \wedge B \wedge C) \tag{1}$$

$$F2 = (\bar{A} \wedge \bar{B} \wedge C) \vee (\bar{A} \wedge B \wedge C) \vee (A \wedge \bar{B} \wedge C) \vee (A \wedge B \wedge C) \tag{2}$$

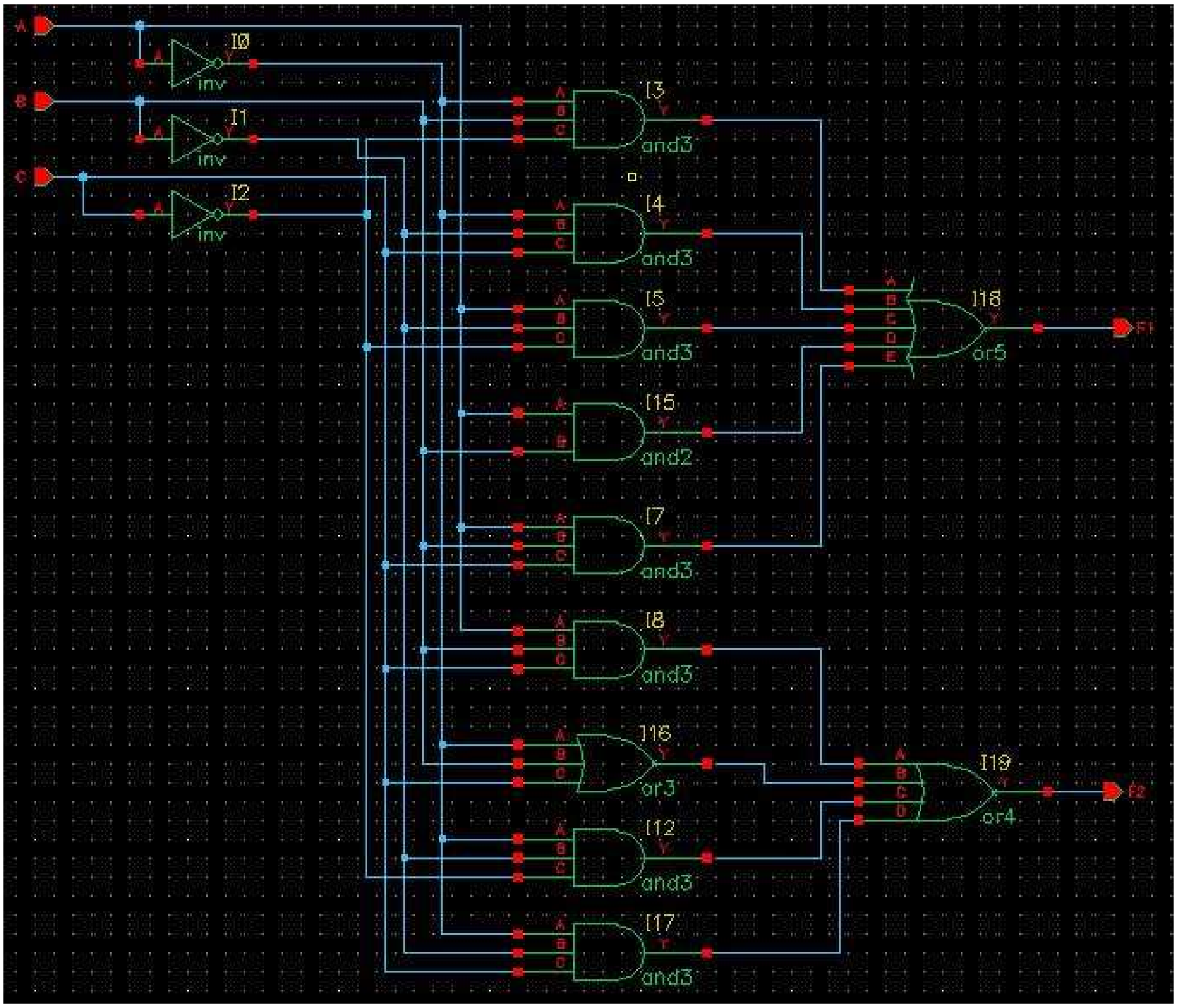

Figure 1: Circuit 3.1.

4 Exercise 3.2

Debugging at drawing phase.

4.1 Exercise 3.2 Tasks

1. Show mistakes and modifications in Figure 1.

5 Exercise 3.3

Debugging after simulation.

Table 2: Truth Table (Specification)

A	B	C	F1
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

5.1 Exercise 3.3 Tasks

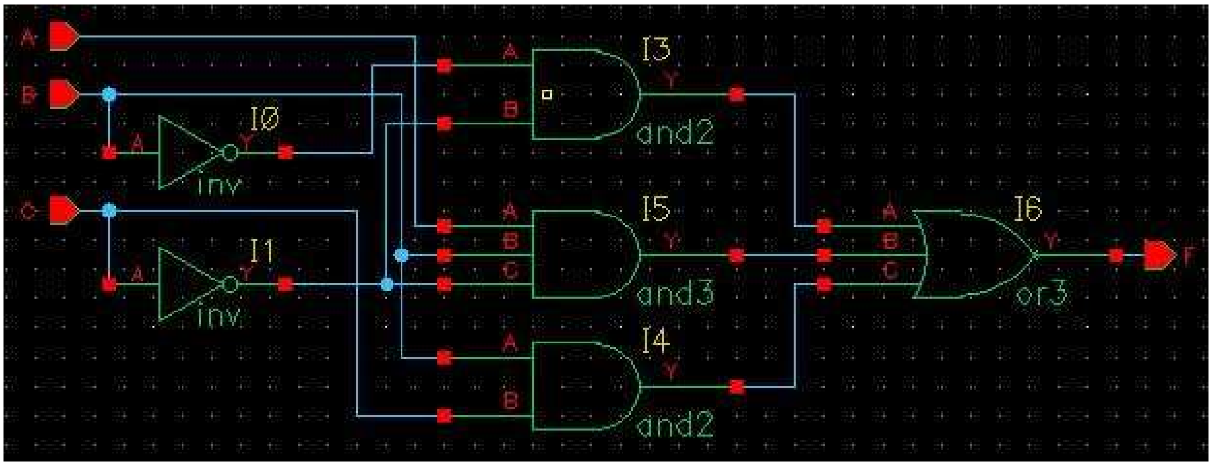

Figure 2: Circuit 3.2.

1. Draw the circuit shown in Figure 2.
2. Simulate the circuit according to the truth table shown in Table 2.
3. When you visulalize the output on *Simvision* tool, you will notice that the output **F** does not satisfy the specification shown in Table 2. Explain when and why **F** is incorrect. You must show incorrect signals for gates I0, I1,and I2 on the waveform. Then, draw the correct circuit and simulate it. Confirm the correctness.

6 Report submission

6.1 Contents

Your report should be prepared in English and should contain the following:

1. Your name, your ID and the Lab #.
2. **Exercise 3.1**

- Show all mistakes in F1 and F2 functions.
- New logic functions.
- New schematic.
- The file $Testfixure.new$ you used for simulation.
- Waveform.
- Show the correctness of the designed circuit.

3. **Exercise 3.2**
   - show all mistakes on the wrong schematic.
   - Write the correct functions on the schematic.
4. **Exercise 3.3**
   - $Testfixure.new$
   - Wrong schematic and waveform.
   - Show when and why F is incorrect on the waveform.
   - New schematic and waveform.
   - Show the correctness of the designed circuit.

6.2 Submission Format

Hard Copy.

References

[1] Hiroshi Saito, Logic Circuit Design Web page, 2008, http://web-int.u-aizu.ac.jp/ hiroshis/classes/LD/top.html