F4 - Logic Circuit Design Exercises

2nd Semester, 2008

Lab 2

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1 Objective

Learn how to simulate basic logic circuits with Verilog-XL simulator.

2 Introduction to Cadence design tool

Read the following tutorial about Cadence tool:
`http://www.u-aizu.ac.jp/~benab/classes/cs/doc/cadence/`

3 Exercise 2.1

Draw the circuit shown in Fig. 1 with Cadence *icds* design tool then simulate it with Verilog-XL.

3.1 Exercise 2.1 Tasks

1. Write the test input sequence in Verilog HDL and save it into "testfixture.new".
2. Simulate the circuit. The input ports AB should have the following values: 00, 01, 10 and 11 respectively.
3. Verify the output and investigate it with SimVision waveform viewer.
4. Make a table containing all input and output ports values.

4 Exercise 2.2

Simulate the circuit you created in Exercise 1.1 (Lab 1).

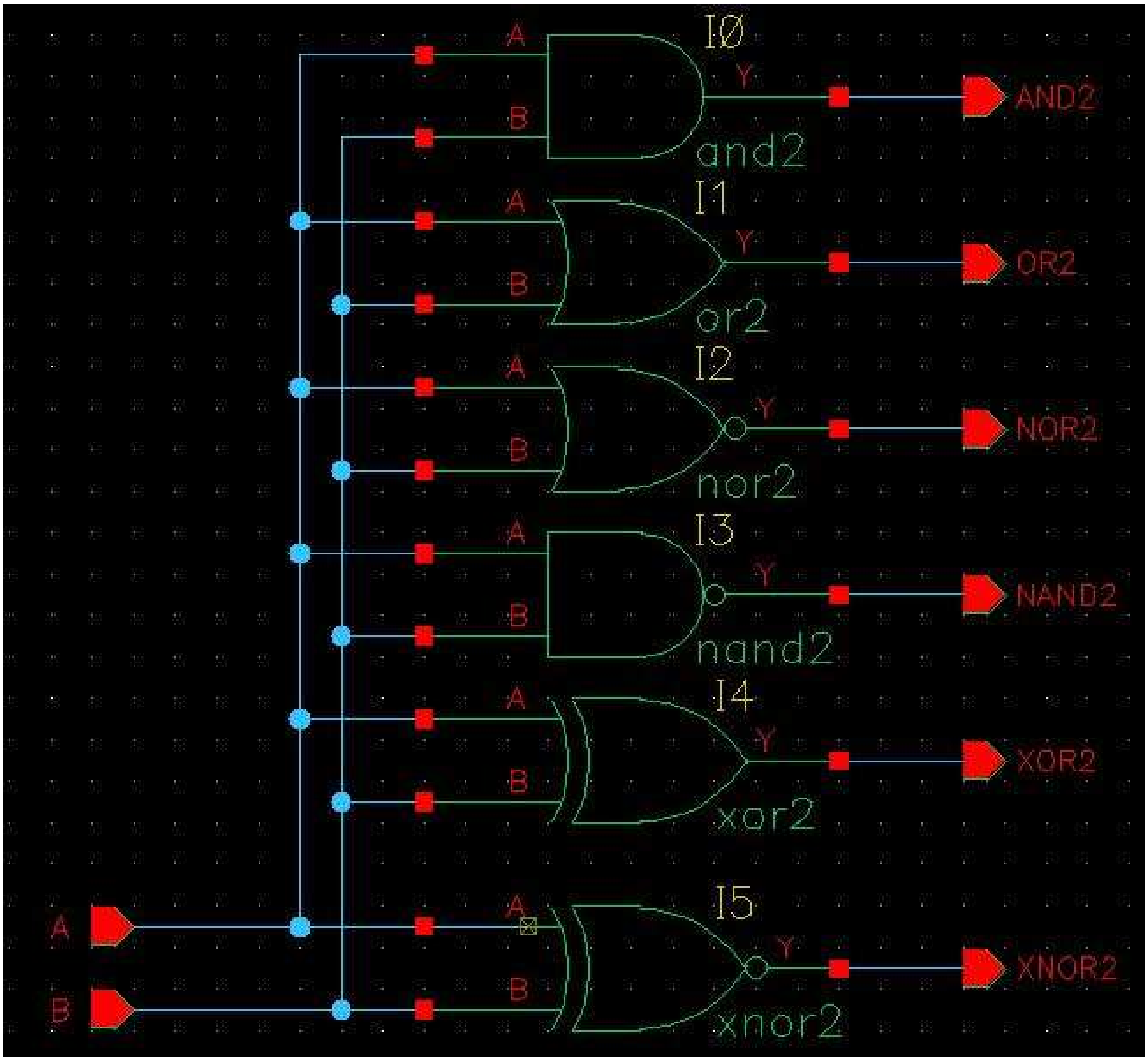

Figure 1: Circuit 2.1.

4.1 Exercise 2.1 Tasks

1. Write a test input sequence in Verilog HDL and name your file: “testfixure.new”
2. Using ”testfixure.new” file, simulate the circuit in Exercise 1.1. with Verilog-XL.
3. Refer to Table 1 and check the correctness of your circuit using Waveform.

5 Exercise 2.3

Simulate the circuit you created in Exercise 1.3 (Lab 1).

5.1 Exercise 2.1 Tasks

1. Write a test input sequence in Verilog HDL and name your file: “testfixure.new”. Refer to Fig 2

Table 1: Truth Table for full Adder

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 2: Truth Table for 4-bit full Adder

A	B	Cin	Sum	Cout
0000	1111	1		
0010	0110	1		
1010	1010	1		
1100	1111	1		
1111	1010	0		
1010	1010	0		
1110	0011	0		
0010	1010	0		

2. Using ”testfixure.new” file, simulate the circuit in Exercise 1.3. with Verilog-XL.
3. Refer to Table 1 and check the correctness of your circuit using Waveform.

6 Submission procedure and Deadline

Your report should be prepared in English and should contain the following:

1. Your name, your ID and the Lab #.
2. All schematics and waveforms
3. All “testfixure.new” files.
4. The three completed tables.
5. Submission format: Hard copy.

References

[1] Hiroshi Saito, Logic Circuit Design Web page, 2008, http://web-int.u-aizu.ac.jp/ hiroshis/classes/LD/top.html

```
//sample textfixure.new in Verilog HDL

initial
begin
 A=1'b0; //
 B=1'b0;
 Cin=1'b0;
 #100
 Cin=1'b1;
 #100
 A=1'b1;
 Cin=1'b0;
 ...
 ..
..
 $finish  // finish simulation
end       // End test sequence
```

Figure 2: Testfixure sample in Verilog HDL.