F4 - Logic Circuit Design Exercises

2nd Semester, 2008

Lab 1

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Release Date:	Oct. 1st, 2008
Due Date	**:** Oct. 8st, 2008

1 Objective

In this lab, you will learn how to design logic circuits using Cadence icds schematic tool.

2 Introduction to Cadense design tool

Read the following tutorial about Cadence tool:
`http://www.u-aizu.ac.jp/~benab/classes/cs/doc/cadence/`

3 Exercise 1-1: Create circuit schematic

Design the circuit shown in Fig. 1 with Cadence *icds* design tool.

4 Exercise 1-2: Create circuit symbol

Create the symbol for the circuit you designed in Exercise 1-1. Refer to Figure 2.

5 Exercise 1-3: Create circuit schematic

Create the circuit shown in Fig 3.

6 Exercise 1-4: Create circuit symbol

Create the symbol for the circuit you designed in Exercise 1-3. Refer to Figure 4

7 Submission procedure and Deadline

Your report should be prepared in English and should contain the following:

1. Your name, your ID and the Lab #.

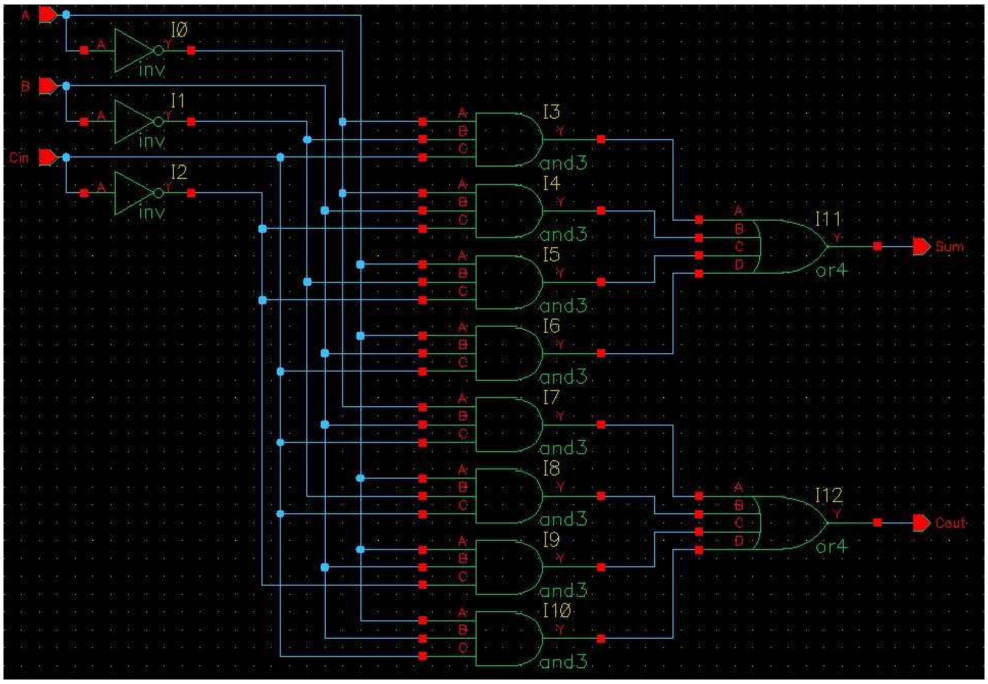

Figure 1: Circuit 1-1.

Figure 2: Symbol for circuit 1-1.

2. All schematics

3. Submission format: Hard copy.

References

[1] Hiroshi Saito, Logic Circuit Design Web page, 2008.

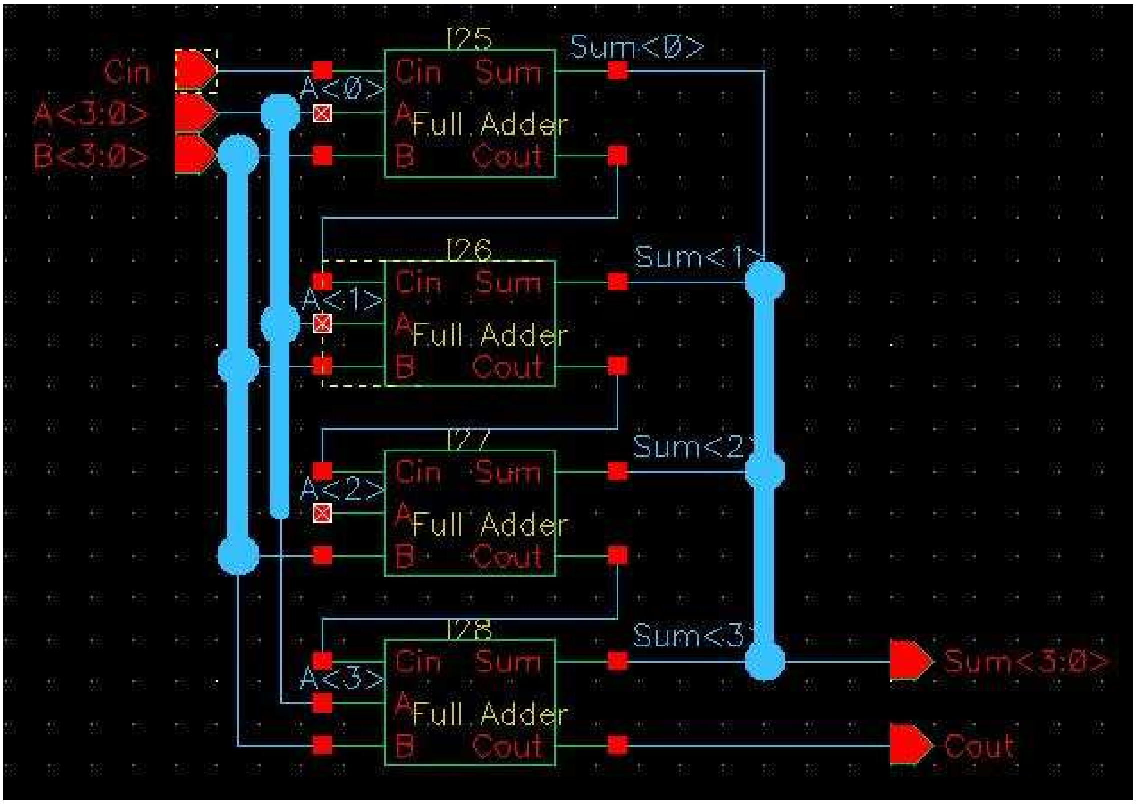

Figure 3: Circuit 1-3.

Figure 4: Symbol for circuit 1-3.